EE 505 Experiment 3
Spring 2023
Clocked Dynamic Comparators

A comparator or multiple comparators is/are invariably the key subcomponents that are used to convert an analog signal to a digital signal in any ADC. Since most data converters are clocked, the comparators are invariably clocked as well. There are several characteristics of a comparator that play a key role in the performance of an ADC but two of the most important characteristics are the offset voltage and the average power dissipation. In this experiment, the performance characteristics of some of the most basic dynamic comparators will be investigated.

Comparators themselves can be grouped into two classes. One class is simply high gain amplifiers that saturate when a sufficiently high differential input is applied. The others have regenerative feedback to cause a latching effect to occur. The high gain amplifiers have small-signal poles in the left half plane and the regenerative feedback structures are almost always designed to have a small-signal pole on the positive real axis. The high gain amplifier types do not necessarily provide a recognized Boolean signal if the differential input is very small. The regenerative structures that have a pole on the positive real axis will are invariably designed to guarantee a valid Boolean output will be obtained provided the output settling interval is long enough. Essentially all comparators are symmetric circuits with an axis of symmetry line that can separate the left half and the right half circuits. Any lack of symmetry in a comparator is a potential contributor to degradation of the offset voltage.

Shown in Fig. 1 is the concept of a latching dynamic comparator. When the switches are on, the comparator is in the EVALUAT state. When the switches are off, the comparator is in the ARM state. Every EVALUATE state must be proceeded by an ARM state in which the comparator is prepared to making a decision when a trigger signal is applied. The trigger signal initiates the transition from the ARM state to the EVALUATE state. For high speed ADCs, the clock rate on the switches can be very high. The switches are, of course, comprised of simple transistors, invariably a single transistor. The buffer on the output is often critical for two purposes, first to obtain Boolean-level compatibility with the following digital circuitry and second, to avoid having the Boolean-circuits (not shown) load the dynamic comparator. Timing on complimentary switches is often critical as may be any skew in delay for same-phase switches.

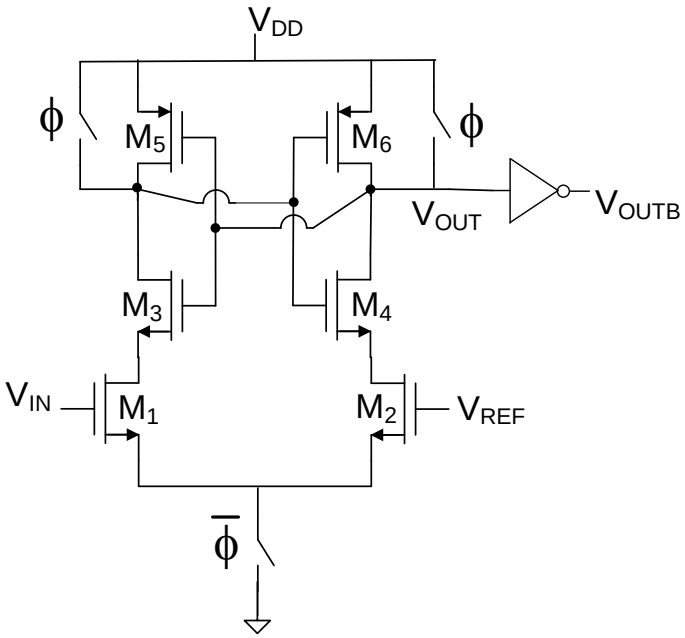

Figure 1: Concept of Basic Dynamic Comparator

Transistor-level implementations of two basic dynamic comparators (buffer not shown) are shown in Fig. 2. The capacitors shown represent any capacitive loading and parasitic capacitances that may be present in the circuit on the output nodes. There may be other parasitic capacitances present as well but these are now shown.

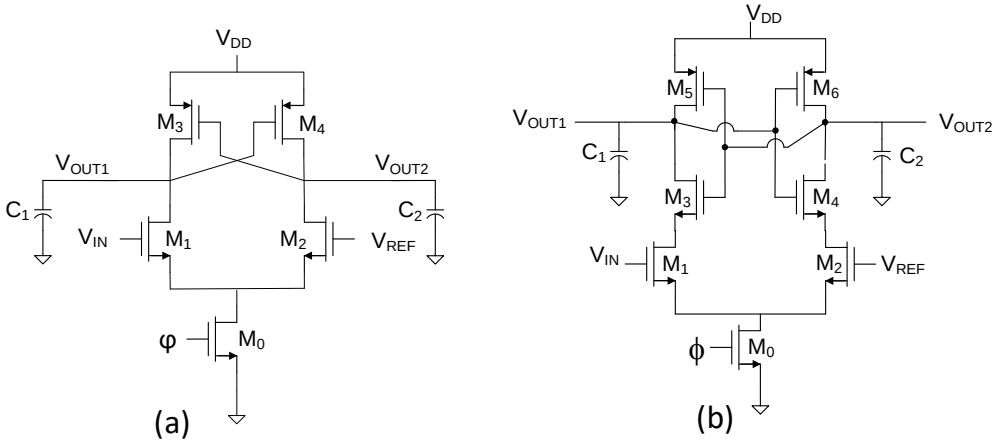

Fig. 2 Two basic simple dynamic comparators

A variant of these two basic dynamic comparators (buffer not shown) is shown in Fig. 3. These structures have pull-up switches that turn on during the ARM state. Though a single-phase clock is shown, the use of n-channel and p-channel switches results in complimentary phasing.

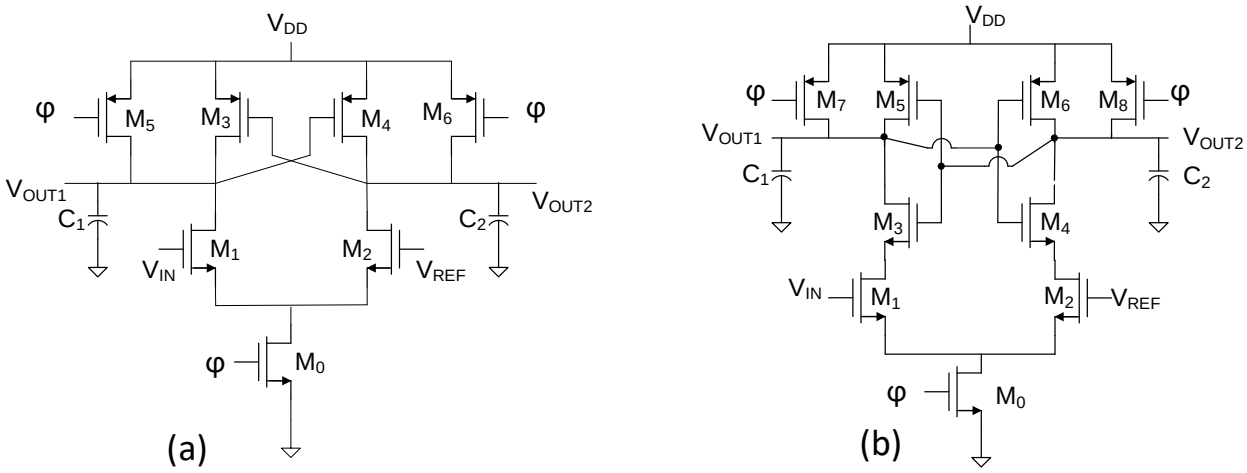

Fig. 3 Two basic dynamic comparators with pull-up outputs

Shown in Fig. 4 are two additional dynamic comparators. The tail voltage switch has been removed in these structures. The circuit of Fig. 4a has two added switch transistors, M_9 and M_{10}.

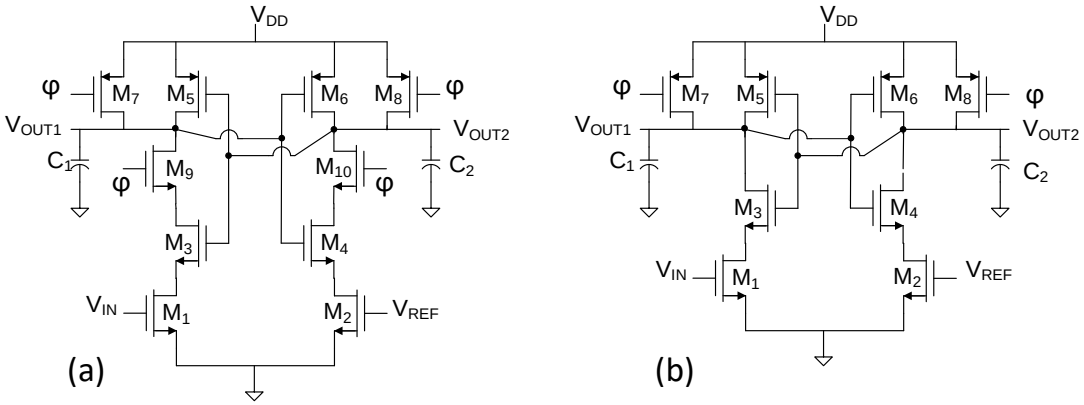

Fig. 4 Two additional dynamic comparators

Experimental Tasks

Task 1.

Design the two circuits in Fig. 2 (i.e. specify device sizes). You may want to consider two implementations, one with a relatively small amount of area in the matching critical components and the other with a significantly larger area in the matching critical components. Compare the offset voltages of the two circuits. In this comparison, identify all factors that you believe will contribute to the offset voltage. Consider the presence or absence of a digital buffer on the left side, the right side, or both when making this comparison. The offset voltage will be dependent upon the clock speed of the comparators. Clearly describe the testbench used for simulating the effects of the offset voltage. Provide computer simulations to predict the offset voltage.

Task 2

Implement the comparator of Fig. 3b in the EDU 1000 and measure the offset voltage. In this implementation, use a supply voltage of V_{DD}=5V. A selection of devices for this comparator in the EDU 1000 is described below. You will need two EDU 1000's to realize this circuit. The two EDU 1000's are distinguished with the presence or absence of a letter "A" in the pin designations. Clearly identify the test bench used for measuring the offset voltage so that you have confidence that the offset voltage you measure represents the actual offset voltage of your comparator. How does the offset voltage change with clock speed?

Task 3

Study the comparators of Fig. 3b and Fig. 4a and comment on how the offset voltage of these comparators should compare to that of Fig. 2b.

EDU 1000

The data for the EDU 1000 is linked on the class WEB site. A pin assignment for using two of these parts to build the circuit of Fig. 3b is shown below. Please note that V_{DD} and SUB must be connected.

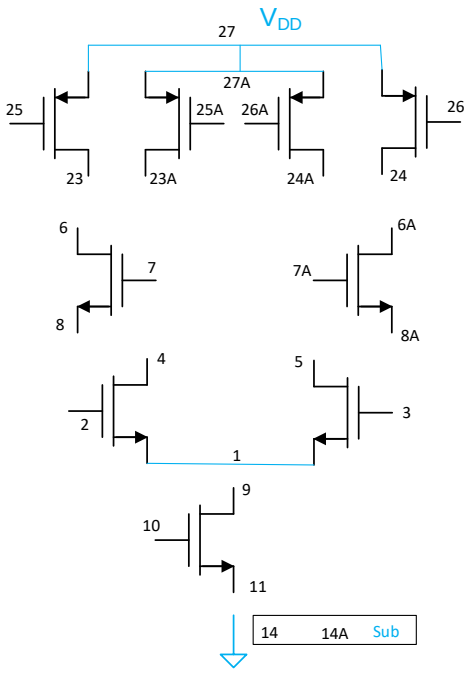

Figure 5: EDU Pin Assignment for Dynamic Comparator of Fig. 3b

The transient response of some of the dynamic comparators discussed in this experiment may look like that shown below. These simulation results are for some specific implementations of the dynamic comparators, not for that of the EDU 1000. Please consider this as for reference only.

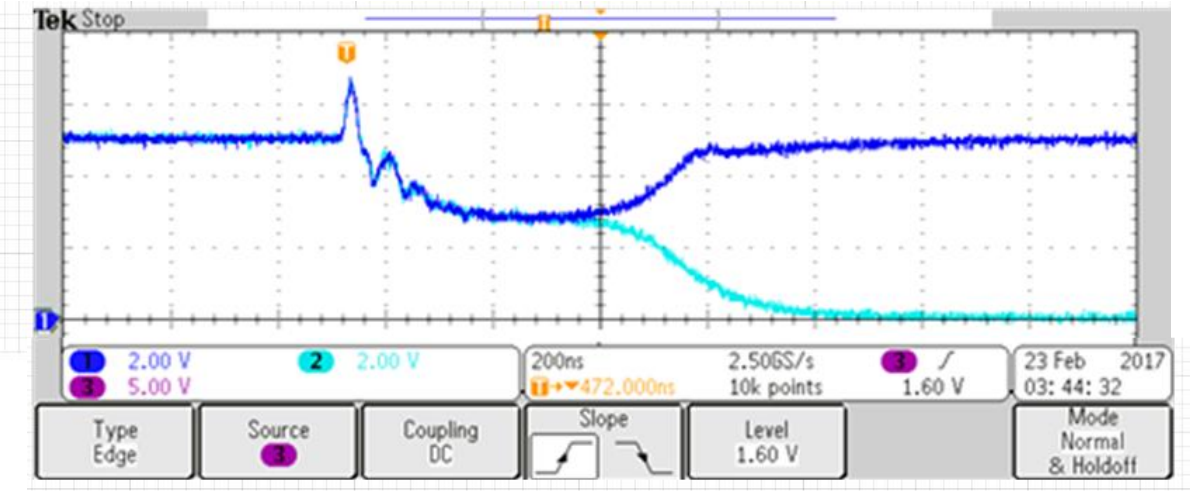

Fig. 6 For reference only, simulated response of dynamic comparator at ARM-EVALUATE Transition

Pin Configuration and Function

N Package
28 Pin DIP
Top View